**Amendments to the Claims**

Claims 1-56 (Canceled).

57. (Previously Presented): A field effect transistor comprising:

a pair of source/drain regions having a channel region positioned there between; and

a gate positioned operatively proximate the channel region, the gate comprising semiconductive material conductively doped with at least one of a p-type or n-type conductivity enhancing impurity effective to render the semiconductive material electrically conductive, a silicide layer and a conductive diffusion barrier layer material effective to restrict diffusion of p-type or n-type conductivity enhancing impurity, the conductive diffusion barrier layer material comprising at least two of $W_xN_y$, $TiO_xN_y$ and $TiW_xN_y$.

58. (Previously Presented): The transistor of claim 57 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiW_xN_y$.

59. (Previously Presented): The transistor of claim 57 wherein the conductive diffusion barrier layer material comprises $TiO_xN_y$ and $TiW_xN_y$.

60. (Previously Presented): The transistor of claim 57 wherein the conductive diffusion barrier layer material is formed over the silicide layer.

61. (Previously Presented): The transistor of claim 57 wherein the silicide layer is formed over the conductive diffusion barrier layer material.

62. (Currently Amended): Integrated circuitry comprising:

a substrate comprising a field effect transistor including a gate, a gate dielectric layer, source/drain regions and a channel region ~~received within a common cross section of the substrate~~; the gate comprising gate semiconductive material conductively doped with a conductivity enhancing impurity of a first type and a conductive diffusion barrier layer material effective to restrict diffusion of first or second type conductivity enhancing impurity; the gate semiconductive material conductively doped with a conductivity enhancing impurity of a first type; the conductive diffusion barrier layer material, the gate dielectric layer, the source/drain regions and the channel region comprising respective cross sectional portions which are received within a common cross section; the conductive diffusion barrier layer comprising at least one of a metal and a metal compound; and

insulative material received proximate the gate within the common cross section, a contact structure extending through the insulative material to the gate and including a portion received within the common cross section, the contact structure including semiconductive material within the common cross section provided in electrical connection with the gate, the semiconductive material provided through the insulative material within the common cross section being conductively doped with a conductivity enhancing impurity of a second type, the conductive diffusion barrier layer material of the gate within the common cross section being provided

between the gate semiconductive material and the semiconductive material provided through the insulative material within the common cross section.

63. (Previously Presented): The integrated circuitry of claim 62 wherein the first type is n and the second type is p.

64. (Previously Presented): The integrated circuitry of claim 62 wherein the first type is p and the second type is n.

65. (Previously Presented): The integrated circuitry of claim 62 wherein the gate also comprises a conductive silicide.

66. (Previously Presented): The integrated circuitry of claim 65 wherein the silicide and the conductive diffusion barrier layer material comprise the same metal.

67. (Previously Presented): The integrated circuitry of claim 62 wherein the semiconductive material within the insulating material contacts the conductive diffusion barrier layer material of the gate.

68. (Previously Presented): The integrated circuitry of claim 62 wherein the semiconductive material within the insulating material does not contact the conductive diffusion barrier layer material of the gate.

69. (Previously Presented): The integrated circuitry of claim 62 wherein the gate also comprises a conductive silicide, the semiconductive material within the insulating material contacting the silicide.

70. (Previously Presented): The integrated circuitry of claim 62 wherein the conductive diffusion barrier layer material is received over the gate semiconductive material, and the semiconductive material within the insulating material is received over the gate.

71. (Previously Presented): The integrated circuitry of claim 62 wherein the insulative material comprises an opening within which the semiconductive material therein has been provided, the opening being substantially void of any conductive diffusion barrier layer material.

72. (Previously Presented): The integrated circuitry of claim 62 wherein the conductive diffusion barrier layer material comprises a material selected from the group consisting of $W_xN_y$, $TiO_xN_y$, and $TiW_xN_y$, and mixtures thereof.

73. (Previously Presented): The integrated circuitry of claim 72 wherein the conductive diffusion barrier layer material comprises $W_xN_y$.

74. (Previously Presented): The integrated circuitry of claim 72 wherein the conductive diffusion barrier layer material comprises $TiO_xN_y$.

75. (Previously Presented): The integrated circuitry of claim 72 wherein the conductive diffusion barrier layer material comprises $TiW_xN_y$.

Claims 76 and 77 (Canceled).

78. (Previously Presented): The integrated circuitry of claim 65 wherein the conductive diffusion barrier layer material is formed over the silicide layer.

79. (Previously Presented): The integrated circuitry of claim 65 wherein the silicide layer is formed over the conductive diffusion barrier layer material.

80. (Previously Presented): The integrated circuitry of claim 62 wherein the gate includes opposing sidewalls in at least one cross section, the contact structure have opposing sidewalls in the one cross section, at least one of the contact structure sidewalls not aligning with either of the opposing sidewalls of the gate in the one cross section.

81. (Previously Presented): The integrated circuitry of claim 62 wherein the gate includes opposing sidewalls in at least one cross section, the contact structure have opposing sidewalls in the one cross section, neither of the contact structure sidewalls aligning with either of the opposing sidewalls of the gate in the one cross section.

82. (Previously Presented): The integrated circuitry of claim 62 wherein the conductive diffusion barrier layer material comprises at least two of $W_xN_y$, $TiO_xN_y$ and $TiW_xN_y$.

83. (Previously Presented): The integrated circuitry of claim 82 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiW_xN_y$.

84. (Previously Presented): The integrated circuitry of claim 82 wherein the conductive diffusion barrier layer material comprises $TiO_xN_y$ and $TiW_xN_y$.

85. (Previously Presented): The integrated circuitry of claim 62 wherein the gate is defined by a single conductive region consisting of a) the conductively doped semiconductive material of the first type, and b) the conductive diffusion barrier layer material.

86. (Previously Presented): The integrated circuitry of claim 85 wherein the conductive diffusion barrier layer material comprises at least two of $W_xN_y$, $TiO_xN_y$ and $TiW_xN_y$.

87. (Previously Presented): The integrated circuitry of claim 85 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiW_xN_y$.

88. (Previously Presented): The integrated circuitry of claim 85 wherein the conductive diffusion barrier layer material comprises $TiO_xN_y$ and $TiW_xN_y$.

89. (Previously Presented): The integrated circuitry of claim 62 wherein the gate is defined by a single conductive region consisting of a) the conductively doped semiconductive material of the first type, b) the conductive diffusion barrier layer material; and c) a conductive silicide.

90. (Previously Presented): The integrated circuitry of claim 89 wherein the conductive diffusion barrier layer material comprises at least two of $W_xN_y$, $TiO_xN_y$ and $TiW_xN_y$.

91. (Previously Presented): The integrated circuitry of claim 89 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiW_xN_y$.

92. (Previously Presented): The integrated circuitry of claim 89 wherein the conductive diffusion barrier layer material comprises $TiO_xN_y$ and $TiW_xN_y$.

93. (Previously Presented): The field effect transistor of claim 57 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiO_xN_y$.

94. (Previously Presented): The integrated circuitry of claim 82 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiO_xN_y$.

95. (Previously Presented): The integrated circuitry of claim 86 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiO_xN_y$.

96. (Previously Presented): The integrated circuitry of claim 90 wherein the conductive diffusion barrier layer material comprises $W_xN_y$ and $TiO_xN_y$.